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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/759,373	01/15/2004	Elias Gedamu	200210154-1	9902

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EXAMINER	
KERVEROS, JAMES C	

ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 12/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/759,373	GEDAMU, ELIAS	
	Examiner	Art Unit	
	JAMES C. KERVEROS	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☒ Claim(s) *2,4,11 and 14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/15/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This is a non-Final Office Action in response to the present US Application 10/759,373, filed 01/15/2004. Claims 1-17 are presently under examination and pending in the Application.

Claim Objections

Claims 2, 4, 11, 14 are objected to because of the following informalities:

Claims 2, 4, 11, 14 recite "was able to execute" should be changed to --to execute--. Appropriate correction is required.

Specification

The abstract of the disclosure is objected to because of legal phraseology, "comprises" and "means". The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details. Correction is required. See MPEP § 608.01(b).

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: "Cache-testable processor identification method and system for performing cache yield analysis".

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Vigil et al. (US Patent 5,732,209), issued: March 24, 1998.

Regarding independent Claims 1, 8, 13, 17, Vigil discloses a method and a system for self-testing a multi-processor die 10 on a wafer, (Figs. 1, 2 and 8), comprising:

Testing a CPU core on a die, Fig. 2, including the step 26 of testing RAM memory arrays in the CPU core, where in some embodiments the RAM arrays tested are in the shared portions of the die, such as the shared level-2 cache. At step 36, during burn-in the CPU core is continuously tested and accumulating errors in the chip. At step 37, the test is completed and a signature generated from the functional test is placed on the chip's I/O pins and read by the external tester, which compares the generated signature to an expected signature to determine if the functional test detected an error. The next CPU core can be tested following the same steps, above. The signature generated from the functional test containing the accumulated errors in the chip corresponds to the claimed file that contains test results for a wafer.

Identifying one of the CPU cores present on the die using an external tester in which the cache array step 26 has passed a cache test. When three or more CPU cores are present on the die, the results from the three CPU cores can be used to "vote" to determine which CPU core is faulty. When the signatures from both CPU cores match for all test results, it can safely be assumed that both cores are good, thus indicating a cache array associated with a CPU has passed a cache test.

Regarding Claims 2-4, 10-12, 14, identifying that a built-in-self-test (BIST) engine is able to execute the cache test, when the signatures from both CPU cores match for all test results. When all results match from each CPU core 14, 16, 17, then no error is detected for the current result being written. When a mis-match occurs, an accumulated error latch is set in self-test controller 50 for the mismatching CPU core. Each data result written out to second-level shared cache 12 can be checked by comparing the three results from the three CPU cores and using voting to determine which CPU core is defective. Anytime a mismatch occurs, either from result comparator 94, or from comparing the internal test points (step 116) or comparing the serial scan chains (step 124), an error is signaled by asserting the self-test result signal. The external tester can then halt testing and move on to the next die on the wafer, Fig. 9.

Regarding Claims 5-7, 9, 15, 16, parsing, opening and decompressing the compressed signatures in the external tester.

Pertinent Art

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Balkin et al. (US Patent No: 5,835,504), issued: November 10, 1998. Balkin discloses a method for a wafer level testing of cache arrays, block 21, including BIST cache testing and fault correction subsequent to wafer dicing, block 25, the processor initiating built-in self test (BIST) at power-up, as shown in Fig. 2.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C. KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JAMES C KERVEROS
Primary Examiner
Art Unit 2138

12/5/06

Date: 5 December 2006
Office Action: Non-Final

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